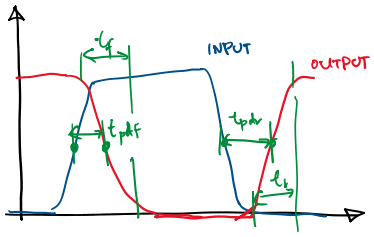
Delay

October 10, 2019 18:23



RISE TIME - (t_r, t_{LH}) time taken from 10% to 90%.
FALL TIME - (t_f, t_{HL}) time taken from 90% to 10%.
EDGE RATE - (t_{rf}) average of rise & fall

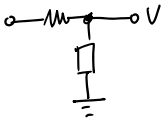
RISE PROPAGATION DELAY (t_{plr}, t_{pLH})
- max. time from input crossing 50% to output crossing 50%

FALL PROPAGATION DELAY (t_{plf}, t_{pHL})
- max. time from input crossing 50% to output crossing 50%

PROPAGATION DELAY (t_{pd})
- average

CONTAMINATION DELAY
- fastest input 50% → output 50%

Recall First Order Circuits

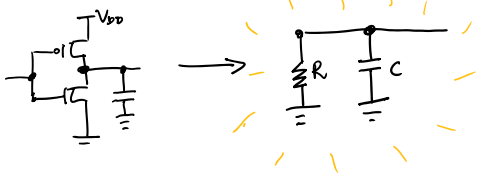


$$V(t) = V_f + (V_i - V_f)\cdot e^{-\frac{t}{\tau}}$$

we need these to describe the circuit

Pull Down: Suppose for $t=-\infty$, input is off, then PMOS pulls output up to 0, and assume at $t=0$, input switch to 1

We can model the MOS as resistor & capacitor:

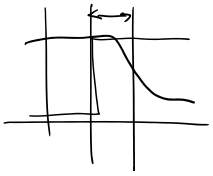


t_{pLH} is time to half: $\frac{V_{DD}}{2}$

$$\frac{V_{DD}}{2} = V_{DD}\cdot e^{-\frac{t}{\tau}}$$

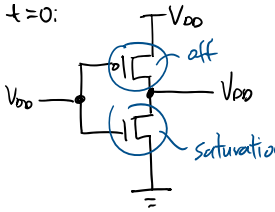
$$\frac{1}{2} = e^{-\frac{t}{RC}}$$

$$t = RC\cdot \ln(2)$$



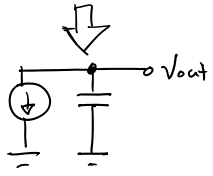
Effective Resistance Calculation

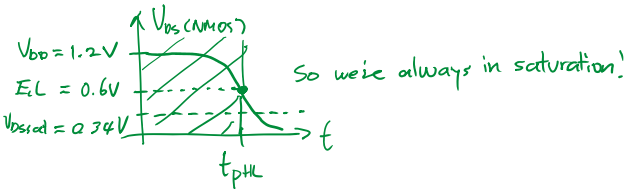
at $t=0$:



Suppose $V_{DD} = 1.2V$, $V_T = 0.4V$, $E_cL = 0.6V$ } $V_{DS_{sat}} = (V_{GS} - V_T)\,//\,E_cL = 0.34V$

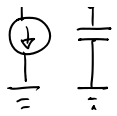
→ so what happens?

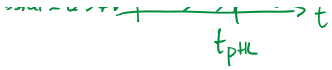




So we're always in saturation!

$$I_{DS} = C_L\cdot\frac{\Delta V}{\Delta t}$$





$$I_{DS} = C_L \cdot \frac{\Delta V}{\Delta t}$$

$$= C_L \cdot \frac{\left(V_{DD} - \frac{V_{DD}}{2}\right)}{t_{pHL}}$$

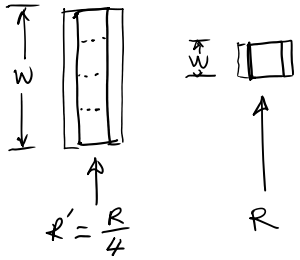
$$I_{DS} = \frac{C_L \cdot V_{DD}}{2 \cdot t_{pHL}} \qquad t_{pHL} = 0.7RC_L \text{ also}$$

$$t_{pHL} = 0.7RC_L = \frac{C_L \cdot V_{DD}}{2 \cdot I_{DS}}$$

$$\Downarrow$$

$$R = \frac{V_{DD}}{1.4\, I_{DS}} \leftarrow \text{effective resistance}$$

Note: (This) calculation is for unit transistor ($W = L$), If W is larger, then resistance is smaller



Note: Resistance of PMOS is typically (~2.5×) higher because mobility of holes (for PMOS) is much smaller.

The size of PMOS is bigger than NMOS is so that V_S is around the middle (recall W_N & W_P determines X)

from example:

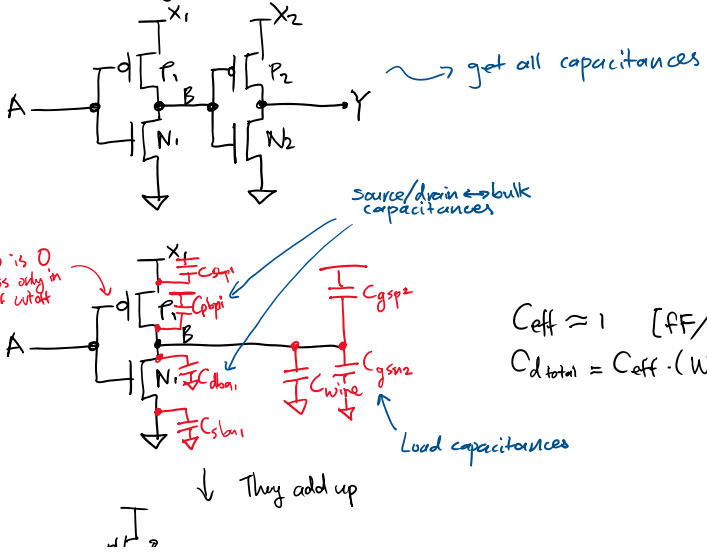
$$R_{eq} = \frac{(Vdd/2)}{0.7 \times I_{sat}}$$

$$R_{eqn} = \frac{(Vdd/2)}{0.7 \times I_{sat}} \quad (L = W)$$

$$R_{eqp} = \frac{(Vdd/2)}{0.7 \times I_{sat}} \quad (L = W)$$

R_{eq}, R_{eqn}, R_{eqp} $\propto$ to ratio $\frac{L}{W}$ $\rightarrow R_{eq} = R_\square \times \frac{W}{L}$ (typically 3.5)

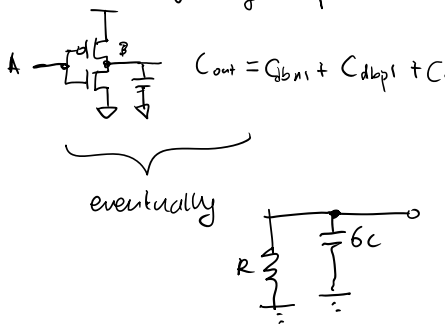
Ex. inverter driving inverter



$$C_{eff} \approx 1 \quad [fF/\mu m]$$

$$C_{d\,total} = C_{eff} \cdot (W_N + W_P)$$

↓ They add up

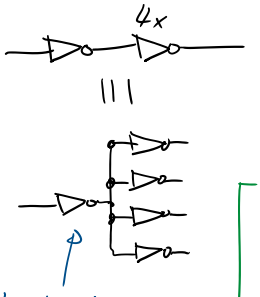


$C_{out} = C_{dbn1} + C_{dbp1} + C_{wire} + C_{gsn2} + C_{gsp2}$

Ex. CMOS inverter has PullUp: $8\lambda : 2\lambda$, $2\lambda = L = 200nm$, $\lambda = 100nm$.
Pull Down: $4\lambda : 2\lambda$

Compute inverter delay using 0.18mm tech. Assume ramp input & $C_{wire} = 0$

Inverter driving 4x identical inverters:



STANDARD VALUES FOR GATE CAPACITANCES:

$C_g = \begin{cases} 2 fF/\mu m & \text{if } 90nm \uparrow \\ 1 fF/\mu m & \text{if } 65nm \downarrow \end{cases}$

$C_G = 2fF/\mu m \cdot (4)(400nm + 800nm) = 9.6fF$ (C_g)

$C_d = 1fF/\mu m \cdot (400nm + 800nm) = 1.2fF$ (C_{eff})

$C_{output} = C_G + C_d = 10.8fF$

STANDARD VALUES FOR NMOS & PMOS EFFECTIVE RESISTANCES

$R_{NMOS} = 12.5k\Omega \times \frac{L}{W} = 6.25k\Omega$ (NMOS Reff)

$R_{pmos} = 30k\Omega \times \frac{L}{W} = 7.5k\Omega$ (PMOS Reff)

$t_{pHL} = (6.25k\Omega)(10.8fF) = 67.5\ ps$

$t_{pLH} = (7.5k\Omega)(10.8fF) = 81.0\ ps$