Design of CMOS Inverter

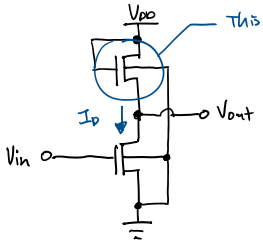
October 8, 2018 17:46

(Noise-margin-centric approach)

Recall components connected to the source is the DRIVER
ground is the LOAD

- Resistors are large & undesirable for implementation

Saturation-Enhanced: Transistors driven by another transistor in saturation



This is on if $V_{out} > V_{DD} + V_T$
off if $V_{out} < V_{DD} + V_T$ ⇒ V_{out} is bounded on upper end

$$V_{OH} = V_{DD} - V_T(V_{OH})$$

↑ function b/c top MOS V_S is not 0

$$V_{OH} = V_{DD} - \left(V_{T0} + \gamma \left(\sqrt{V_{OH} + 2|\phi_F|} - \sqrt{2|\phi_F|} \right) \right)$$

If we're using iterative process, we can start with $V_{OH} \approx V_{DD}$

To find V_{OH}, equate the current

$$I_{D_I}(lin) = I_{D_L}(sat)$$

I for inverting device
L for load device

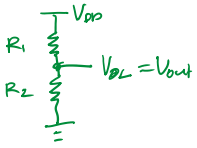
↑ top MOS always in Sat.

V_{OUT}

$$\frac{W_I}{L_I} \cdot \frac{\mu_n C_{ox}}{\left(1 + \frac{V_{out}}{E_{CN} L_I}\right)} \cdot \left((V_{DD} - V_{T_I}) V_{out} - \frac{V_{out}^2}{2} \right) = \frac{W_L v_{sat} C_{ox} (V_{DD} - V_{out} - V_{TL})^2}{(V_{DD} - V_{out} - V_{TL}) + E_{CN} L_L}$$

Ratio of Width of two devices: $K_R = \frac{W_I / L_I}{W_L / L_L}$

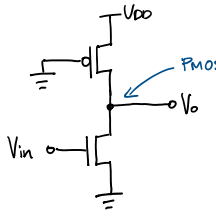
↳ can be modeled as voltage divider



If we want lower V_{OL}, R_2 should be smaller
⇓
inverting MOS width must be bigger.

Pseudo-NMOS Inverter

↳ using a PMOS like a NMOS — forcing gate to V_{DD} or GND



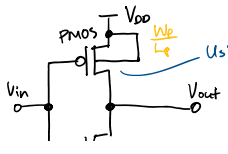
PMOS can pull V_{OH} all the way up to V_{DD}

$$\frac{W_p v_{sat} C_{ox} (V_{DD} - |V_{Tp}|)^2}{(V_{DD} - |V_{Tp}|) + E_{cp} \cdot L_p} = \frac{W_N}{L_N} \cdot \frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{CN} \cdot L_N}\right)} \cdot \left((V_{DD} - V_{TN})(V_{OL}) - \frac{(V_{OL})^2}{2} \right)$$

$$\Rightarrow V_{OL} = \frac{I_{DP}(sat)}{k_N (V_{DD} - V_{TN})}$$

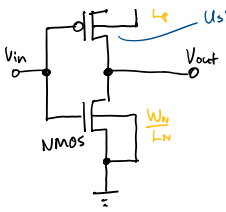
DISADVANTAGE: LOW → HIGH propagation is a lot longer
← Because PMOS has lower mobility
← Because hole mobility is lower than electron mobility
← and PMOS is small
→ so resistance is high
→ so time constant for pulling ↑ is large
→ so delay is longer

CMOS Inverter



Using PMOS, so $V_{OL} = V_{DD}$ (no V_T)

Essentially NMOS & PMOS is fighting,
Vin will determine which one is more dominating



Using PMOS, so $V_{OL} = V_{DD}$ (no V_T)

Essentially NMOS & PMOS is fighting,
V_{in} will determine which one is more dominating

↑
"Who is winning" depends on the SWITCHING POINT (V_S)

To find V_S, we equate top current w/ bottom current. ⟶

$$\frac{W_N v_{sat} C_{ox} (V_S - V_{TN})^2}{(V_S - V_{TN}) + E_{cN} \cdot L_N} = \frac{W_P v_{sat} C_{ox} \cdot (V_{DD} - V_S - |V_{TP}|)^2}{(V_{DD} - V_S + |V_{TP}|) + E_{cP} \cdot L_P}$$

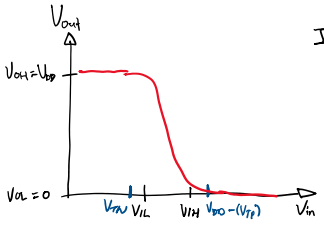
Both MOS are in Saturation.
- ← Because at V_S, $V_{in} = V_{out}$
- → So $V_D = V_G$
- → So $V_{DS} = V_{GS}$
- → So $V_{GS} < V_{DS} - V_T$
- → So saturation

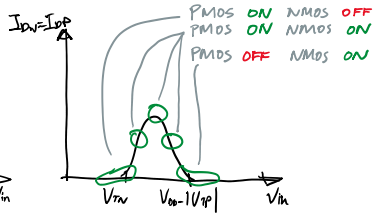
Assign $X = \sqrt{\frac{W_N E_{cP} L_P}{W_P E_{cN} L_N}} = \sqrt{\frac{W_N E_{cP}}{W_P E_{cN}}}$

But also $X = \frac{V_{DD} - V_S - |V_{TP}|}{V_S - V_T}$ (ratio of "strength" of PMOS vs. NMOS)

$$\Downarrow$$

$$V_S = \left(\frac{V_{DD} - |V_{TP}| + X V_{TN}}{1 + X} \right)$$





* If $W_N > W_P$ ($\uparrow X$), we shift the V_S left (←)
* If $W_P > W_N$ ($\downarrow X$), we shift the V_S right (→)