Mini Project 3

Multi-Transistor Amplifiers

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November 10, 2017

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0 Introduction

In this mini-project, we will experiment with multi-transistor amplifiers. In particular, the Cascode amplifier, the cascaded amplifier, and the differential amplifier. CircuitMaker software will be used to simulate circuits and models. Excel will be used for other analysis.

1 Part 1: Cascode Amplifier

For this part, we want to built a Cascode amplifier using one common-base amplifier setup and one common-emitter amplifier setup. The requirements are as follows:

- R_{out} is maximum of 5kΩ at midband
- R_{in} is in the range of 5k$Omega$ to 10k$Omega$ at midband
- $|A_V|$, the absolute voltage gain, is at least 50 at midband
- f_L, the low frequency cut-in frequency, is maximum of 500Hz

Finding Resistances

We also know that we are supplying V_{CC}=10V and the base capacitor, C_B is 100μF. We assume that V_{BE} for the transistors are 0.7V. Also from the previous mini-project[5], we know that the β or h_{fe} is approximately 167. We shall use the 1/4 rule to bias the Cascode amplifier as shown in figure 1. Thus,

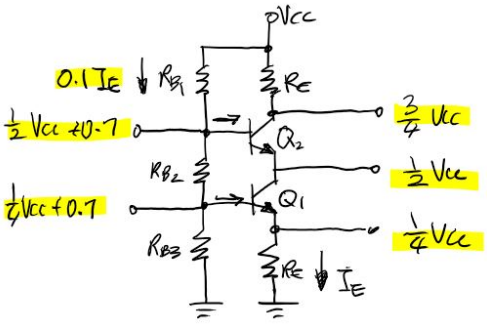


Figure 1: 1/4 rule for biasing Cascode amplifiers

$$V_{C2} = \frac{3}{4}V_{CC} = \boxed{7.5\text{V}}$$
$$V_{E2} = V_{C1} = \frac{1}{2}V_{CC} = \boxed{5.0\text{V}}$$
$$V_{E1} = \frac{1}{4}V_{CC} = \boxed{2.5\text{V}}$$
$$V_{B2} = V_{E2} + 0.7 = \boxed{5.7\text{V}}$$
$$V_{B1} = V_{E1} + 0.7 = \boxed{3.2\text{V}}$$

Since we want the maximum R_{out} to be less than 5kΩ, and since R_{out} is also just R_C, we can set R_C to be 4.7kΩ standard resistor value for safe measures. Now we can compute all the currents.

$$
\begin{aligned}
I_{C2} &= \frac{10 - 7.5}{4.7\text{k}} = \boxed{0.532\text{mA}} \\
I_{B2} &= \frac{1}{\beta} = \boxed{3.19\mu\text{A}} \\
I_{E2} = I_{C1} &= I_{C2} + I_{B2} = \boxed{0.535\text{mA}} \\
I_{B1} &= \frac{1}{\beta} I_{C1} = \boxed{3.20\mu\text{A}} \\
I_{E1} &= I_{B1} + I_{C1} = \boxed{0.538\text{mA}}
\end{aligned}
$$

Using the 1/4 rule, current that flows through R_{B1} is $0.1I_{E2}$:

$$
\begin{aligned}
I_1 &= 0.1 I_{E1} = \boxed{53.2\mu\text{A}} \\
I_2 &= I_1 - I_{B2} = \boxed{50.0\mu\text{A}} \\
I_3 &= I_2 - I_{B1} = \boxed{46.8\mu\text{A}}
\end{aligned}
$$

Knowing all the currents and voltages, we may compute the resistor values. Let $\rightarrow$ denote choosing the closest standard resistor to be used in a circuit.

$$
\begin{aligned}
R_E &= \frac{2.5\text{V}}{I_{E1}} = 4.65\text{k}\Omega && \rightarrow 4.7\text{k}\Omega \\
R_{B1} &= \frac{10\text{V} - 5.7\text{V}}{I_1} = 80.8\text{k}\Omega && \rightarrow 82\text{k}\Omega \\
R_{B2} &= \frac{5.7\text{V} - 3.2\text{V}}{I_2} = 50.0\text{k}\Omega && \rightarrow 51\text{k}\Omega \\
R_{B3} &= \frac{3.2\text{V}}{I_3} = 68.4\text{k}\Omega && \rightarrow 68\text{k}\Omega
\end{aligned}
$$

Small Signal Parameters

For transistor Q_2, the collector current is I_{C2}=0.532mA, thus the transconductance gain $g_{m_2}=\frac{0.532\text{mA}}{25\text{mV}}$=0.021S and $r_{\pi 2}$ is 7.85kΩ. For transistor Q_1, I_{C1}=0.538mA, so g_{m_1}=0.022S and $r_{\pi 1}$=7.76kΩ. For the sake of simplicity, we will use 7.8kΩfor both r_π since the transistors are identical.

Finding Capacitances

First , we get the low frequency small-signal model circuit (shown in figure 2). We see that C_{C2} is decoupled from the rest of the circuit. The equivalent resistances seen by C_{C2} is R_C+R_L≈55kΩ. Which is quite large, and leads to a relatively low frequency location for the pole it is contributing to.

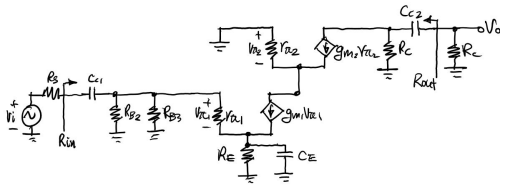


Figure 2: Cascode low frequency small signal model

From previous investigations[5], we know that to be cost efficient, C_{C1} should short first. For this reason, we will conduct OCTC test on C_{C1} and SCTC test on C_E.

$$\begin{aligned}
\tau_{OC}^{C_{C1}} &= C_{C1} \times (R_S + R_{B2} \parallel R_{B3} \parallel (r_{\pi 1} + (1+\beta)R_E)) \\
&= C_{C1} \times 28.2\text{k}\Omega \\
\tau_{SC}^{C_E} &= C_E \times \left(\frac{1}{1+\beta}(R_S \parallel R_{B2} \parallel R_{B3} + r_{\pi 1}) \parallel R_E \right) \\
&\approx C_E \times 50\Omega
\end{aligned}$$

As we can see, the resistances seen by the emitter capacitor is very small comparatively. Thus, C_E capacitor contributes the dominant pole with its location at $\omega_{LP} = \frac{1}{50C_E}$.

There is one zero-not-at-zero. The location of that particular zero is at $\omega_{LZ} = \frac{1}{R_E C_E}$. This might affect the cut-in frequency, so we account for it.

Putting all together and we can compute for C_E given the cut-in frequency:

$$\begin{aligned}
\omega_{L3dB} = 500 \times 2\pi &= \sqrt{\left(\frac{1}{50C_E}\right)^2 - 2\left(\frac{1}{4700C_E}\right)^2} \\
\implies C_E &= 6.37\mu\text{F}
\end{aligned}$$

Setting to standard values, we obtain 6.8µF. We shall also set the coupling capacitors to be the same value.

Having everything put together, we have the following circuit in figure 3.

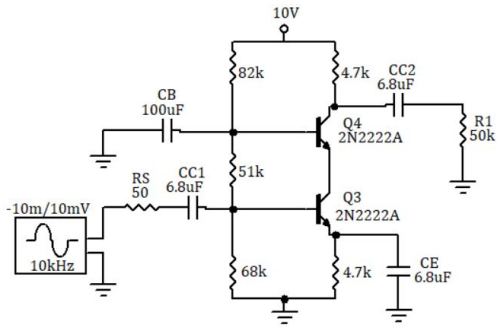


Figure 3: Biased Cascode amplifier

1.1 A - DC Operating Point

	$\mathbf{V_C}$	$\mathbf{V_B}$	$\mathbf{V_E}$	$\mathbf{I_C}$	$\mathbf{I_B}$	$\mathbf{I_E}$
$\mathbf{Q_2}$	7.49V	5.65V	5.07V	534μA	3.49μA	538μA
$\mathbf{Q_1}$	5.07V	3.13V	2.54V	538μA	3.51μA	541μA

Table 1: DC operating point for Cascode amplifier

Based on the circuit built in figure 3, the DC operating values are as shown in table 1.

1.2 B - Frequency Response

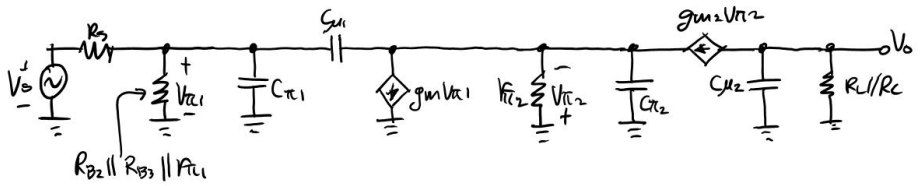
Calculated Frequencies
As established before, capacitors C_{C1} and C_{C2} do not change the low frequency cut-off frequency as much since C_E contributes to the dominant pole. Nevertheless, let C_{C1}, C_E, and C_{C2} be 1, 2, and 3 respectively; the pole and zero locations are calculated as follows.

$$\begin{aligned}
\omega_{Lp1} &= \frac{1}{6.8\mu\text{F} \times 28.2\text{k}\Omega} = 5.2\text{rad}\,\text{s}^{-1} \\
\omega_{Lp2} &= \frac{1}{6.8\mu\text{F} \times 50\Omega} = 2.94\text{krad}\,\text{s}^{-1} \\
\omega_{Lp3} &= \frac{1}{6.8\mu\text{F} \times 55\text{k}\Omega} = 2.7\text{rad}\,\text{s}^{-1} \\
\omega_{Lz1} &= \omega Lz3 = 0 \\
\omega_{Lz2} &= \frac{1}{6.8\mu\text{F} \times 4.7\text{k}\Omega} = 31.3\text{rad}\,\text{s}^{-1}
\end{aligned}$$

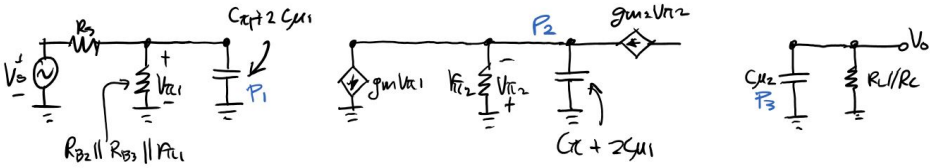
Thus the calculated cut-in frequency is

$$\begin{aligned}
\omega_{L3dB} &= \sqrt{\omega_{Lp1}^2 + \omega_{Lp2}^2 + \omega_{Lp3}^2 - 2\omega_{Lz2}^2} = 2.94\text{krad}\,\text{s}^{-1} \\
f_{3dB} &= \boxed{468\text{Hz}}
\end{aligned}$$

For high-frequency cut-off frequency, we compute the location for the high frequency poles. For which we need the high frequency small-signal model and its Miller equivalence (figure 4a and figure 4b). Also the high-frequency capacitors values are found in the datasheet. Under the current condition, C_{pi} is found to be 18pF and C_μ is found to be 8pF. The poles are calculated as usual.



(a) Cascode high frequency small signal model



(b) Cascode high frequency small signal model after Miller

Figure 4: Cascode circuit at high frequency

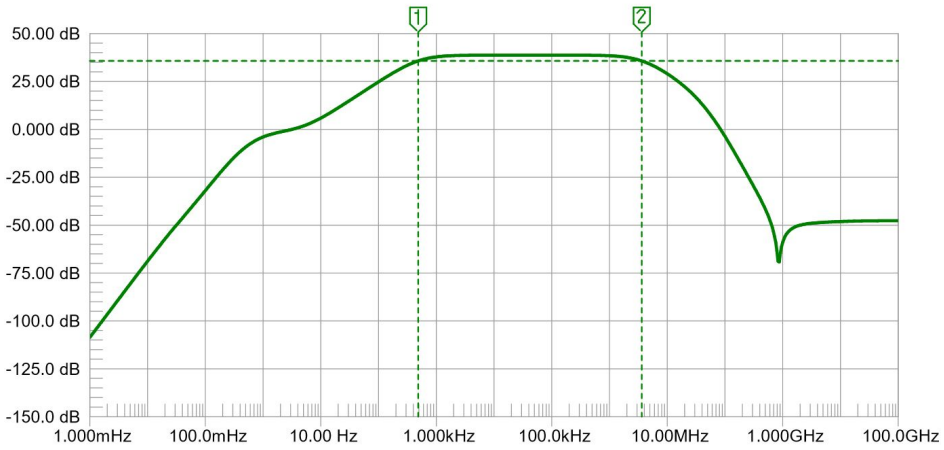
$$\omega_{Hp1} = \frac{1}{(18\text{pF} + 2(8\text{picoF})(50)} = 588\text{Mrad}\,\text{s}^{-1}$$
$$\omega_{Hp2} = \frac{1}{\frac{r_\pi}{1+\beta}(18\text{pF} + 2(8\text{pF}} = 650\text{Mrad}\,\text{s}^{-1}$$
$$\omega_{Hp3} = \frac{1}{8\text{pF}(R_L \parallel R_C} = 29.1\text{Mrad}\,\text{s}^{-1}$$

The high frequency cut-off frequency is then calculated as

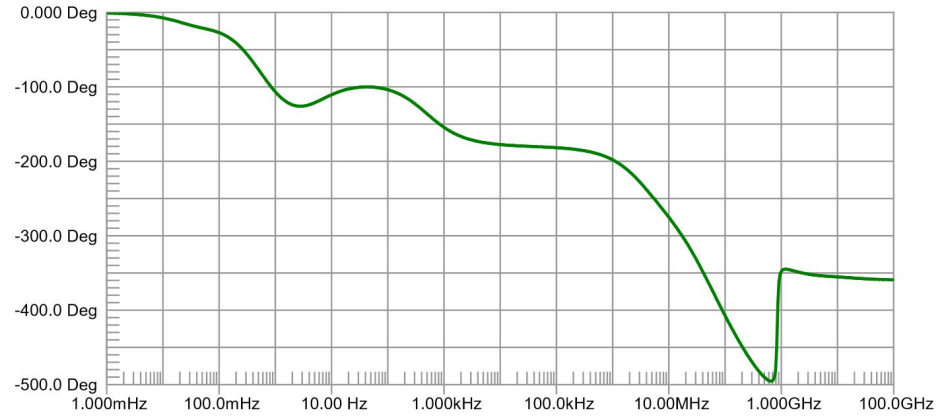
$$\omega_{H3dB} = \sqrt{\tau_{Hp1}^2 + \tau_{Hp2}^2 + \tau_{Hp3}^2}^{-1} = 29.0\text{Mrad}\,\text{s}^{-1}$$
$$f_{H3dB} = \boxed{4.62\text{MHz}}$$

Simulated Frequencies

The bode plot for magnitude and phase is as follows in figure 5



(a) Cascode magnitude bode plot



(b) Cascode phase bode plot

Figure 5: Bode plots for the Cascode amplifier

Measured graphically, the low frequency cut-in frequency is $\boxed{488\text{Hz}}$, and the high frequency cut-off frequency is $\boxed{3.63\text{MHz}}$. The low 3dB frequency is accurate within 4%. However, the high-frequency calculation is very inaccurate, possibly due to Miller.

1.3 C - Saturation

A frequency of 10kHz from mid-band is chosen. Input amplitude is increased from 1mV to 20mV before the output signal gets saturated. Figure 6 depicts the voltage gain versus input voltage amplitude. At the linear region at mid-band the gain, $|A_V|$, is > 85, thus meeting the requirements.

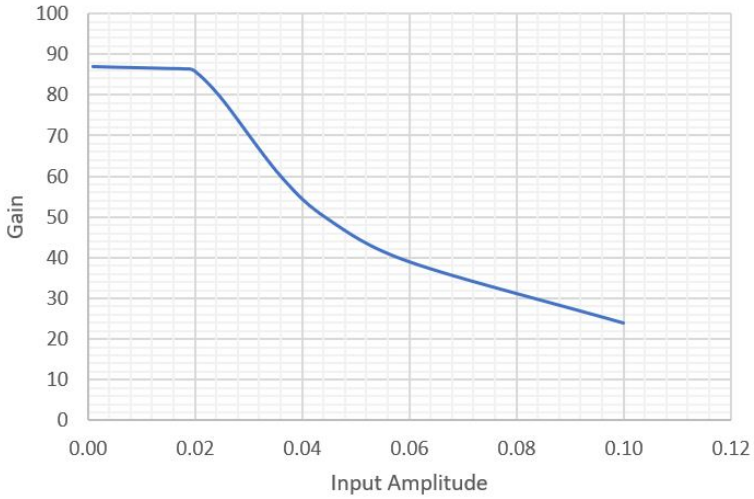


Figure 6: Cascode gain vs. input signal amplitude

1.4 D - Input Output Impedances

Calculated Impedances
The calculations are made easier since input and output is decoupled at mid-band. So, the input impedance is given by:

$$R_{in} = R_{B2} \parallel R_{B3} \parallel r_\pi = 7.3\text{k}\Omega$$

The output impedance is just simply R_C, which is 4.7kΩ.

Measured Impedances
A test current and test voltage is measured at the input and output nodes is used to determine the input and output impedances. R_in is measured to be

$$\frac{702\mu\text{V}}{107\text{nA}} = 6.58\text{k}\Omega$$

Both measured and calculated impedance fall within the requirements. Which is good.

2 Part 2: Cascaded Amplifier

We need to build a common-collector (followed by a common-base) amplifier with an input impedance and output impedances of 50Ω with a tolerance of 5Ω. The 2N3904 NPN transistors are to be used in this exploration. Note that, from previous investigations, 2N3904 has a $h_{fe} = \beta$=164.

2.1 A - Cascaded Biasing

First, let's consider the mid-band small signal model, as seen in figure 7, so that we can construct the equations for input and output impedance.

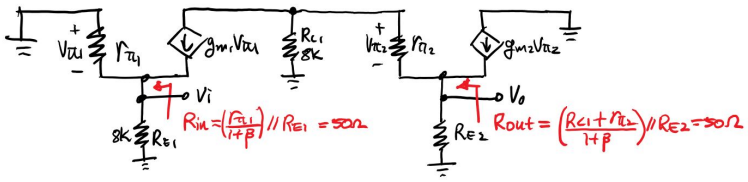


Figure 7: Cascaded amplifier at mid-band

Observe that

$$\begin{aligned} R_{in} &= \frac{r_\pi}{1+\beta} \parallel R_{E1} \\ &= \frac{\beta}{1+\beta}\frac{V_T}{I_{C1}} \parallel \frac{V_{E1}}{I_{E1}} \\ &= \frac{V_T}{I_{E1}} \parallel \frac{V_{E1}}{I_{E1}} \\ &\approx \frac{V_T}{I_{E1}} \end{aligned}$$

Since we want R_{in} to be 50Ω, and assuming V_T=25mV, then I_{E1}=0.5mA.

Knowing this, we can start using the 1/3 rule where $V_{E1}=\frac{1}{3}V_{CC}$ to bias the common-base circuit. The DC circuit is as shown in figure 8. We can bias the common-base using the 1/3 rule since we assume the input impedance of the second transistor is quite large.

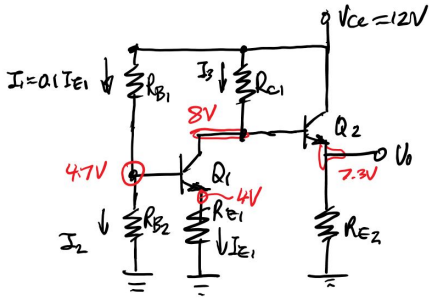


Figure 8: Cascaded amplifier at DC

$$\begin{aligned} V_{E1} &= 4\text{V} \\ V_{B1} &= 4.7\text{V} \\ V_{C1} = V_{B2} &= \frac{2}{3}V_{CC} = 8\text{V} \\ V_{E2} &= V_{B2} - 0.7 = 7.3\text{V} \end{aligned}$$

Thus, $I_1 = 0.1 \times I_{E1} = 50\text{mA}$. Also $I_{B1} = \frac{1}{1+\beta} \times 0.5\text{mA} = 3.03\mu\text{A}$.

It follows that

$$I_2 = I_1 - I_{B1} = 47.0\mu\text{A}, \quad I_{C1} = \beta I_B = 0.497\text{mA}$$

Therefore,

$$R_{E1} = \frac{4}{0.5\text{mA}} = \boxed{8\text{k}\Omega}$$
$$R_{B1} = \frac{12 - 4.7}{50\mu\text{A}} = \boxed{146\text{k}\Omega}$$
$$R_{B2} = \frac{4.7}{47.0\text{mA}} = \boxed{100\text{k}\Omega}$$

Next, we look at the constraint set by the output impedance. It follows this equation:

$$R_{out} = \frac{R_{C1} + r_{\pi_2}}{1+\beta} \parallel R_{E2} = 50$$

Again, rearranging and substituting variables, we yield the equivalent equation

$$50 = \left(\frac{R_{C1}}{1+\beta} + \frac{V_T \times R_{E2}}{V_{E2}}\right) \parallel R_{E2}$$

But simultaneously, we know that $R_{C1} = \frac{12-8}{I_3}$ where $I_3 = I_{C1} + I_{B2}$. We substitute $I_{B2} = \frac{1}{1+\beta} I_{E2}$ and $I_{E2} = \frac{7.3}{R_{E2}}$, and solve for R_{E2}.

$$\implies R_{E2} = \boxed{1.59\text{k}\Omega}$$

It follows that $I_{E2} = \frac{7.3}{1.59\text{k}\Omega} = 4.6\text{mA}$; $R_{C1} = \boxed{7.62\text{k}\Omega}$.

To find capacitances, we look at the low frequency small signal model, shown in figure 9. Since C_{C1} and C_{C2} sees similar resistances, we design these two capacitors to have the same pole locations. This is fine since the two capacitors are decoupled from each other. Let C_B, C_{C1}, and C_{C2} be indexed by 1,2, and 3 respectively.

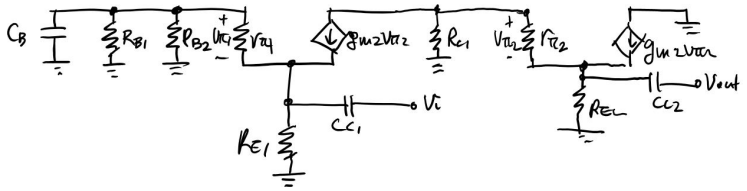


Figure 9: Cascaded amplifier low-frequency small signal model

Look at C_{C2} first,

$$\omega_{Lp3} = \left[\left(\underbrace{\frac{R_{C1} + r_{\pi 2}}{1+\beta} \parallel R_{E2}}_{49.8\Omega}\right) \times C_{C2}\right]^{-1}$$

C_{C2} sees relatively small resistance. Therefore, C_{C2} contributes to a dominant pole. The same could be said for C_{C1} as as we do the SCTC test for it:

$$\tau_{SC}^{C_{C1}} = \left(\frac{1}{1+\beta} r_{\pi 1} \parallel R_{E1}\right) \times C_{C1} = C_{C1} \times 50$$

Therefore, C_{C1} also contributes to the dominant pole.

Now equating to the required low frequency cut-in frequency. Since we treat C_{C1} and C_{C2} the same, we set them to C.

$$1000\text{Hz} = \sqrt{2\left(\frac{1}{C \times 50\Omega}\right)^2}$$
$$\frac{\sqrt{2}}{2000\pi} = 50C$$
$$C = \frac{\sqrt{2}}{10000\pi}$$
$$\implies C_{C1} = C_{C2} = \boxed{4.5\mu\text{F}}$$

The pole locations for these capacitors are

$$\frac{1}{50 \times 4.5\mu\text{F}} = 4.44\text{rad}\,\text{s}^{-1}$$

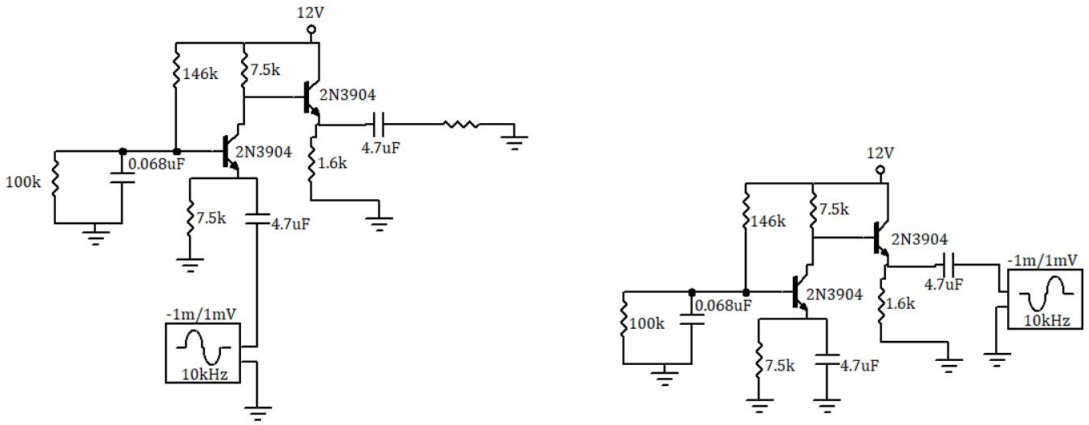
We want the pole contributed by C_B to be at least one decade below for an accurate assumption. Thus, the pole location by C_B must be less than $444\text{rad}\,\text{s}^{-1}$. Furthermore, when we evaluate for C_B, we find that C_B must be less than or equal to 40nF.

2.2 B - Circuit and Impedance

Building the circuit, we standardize the values.

$$R_{E1} = 8.2\text{k}\Omega, \quad R_{B1} = 150\text{k}\Omega, \quad R_{B2} = 100\text{k}\Omega, \quad R_{E2} = 1.6\text{k}\Omega, \quad R_{C1} = 7.5\text{k}\Omega$$
$$C_{C1} = 4.7\mu\text{F}, \quad C_{C2} = 4.7\mu\text{F}, \quad C_B = 0.039\mu\text{F}$$

The built circuit will look like as follows (figure 10).



(a) Cascaded amplifier circuit to measure R_{in} (b) Cascaded amplifier circuit to measure R_{out}

Figure 10: Cascaded amplifier built with standard values

Note that after the circuit is built, C_B changed to 0.068µFin order to bring the 3dB cut-in frequency around but below 1000Hz. Also the input impedance was slightly too high (at 57Ω), so I changed R_{E1} down to 7.5kΩ.

After modification, the input resistance is 51.95Ω and the output impedance is 54.0Ω.

I used the transient analysis to measure the gain of the output signal, which had a V_{PP} of 273mV when supplied with an input of 1mV. Thus, $|A_M|$=136.5.

2.3 C - Attaching Input and Output Impedances

Input and output impedance of both 50Ω are added. The cut-in frequency is now 670Hz, which is a bit too low. The cut-out frequency is 3.43MHz.

In order to meet requirements better, I adjusted C_B to 0.027µFsuch that the cut-in frequency is closer but not exceeding 1000Hz.

The new cut-in frequency is 946Hz.

3 Part 3: Differential Amplifier

Using the steps learned in class, the differential amplifier is set up as in figure 11. A current mirror is used to obtain a more accurate simulation of the real amplifier. Since the emitter current of the two 2N3904 BJTs are both 0.5mA, we need to pull a total of 1.0mA using the current mirror.

$$I_{ref} = I_o \left(1 + \frac{1}{\beta}\right)$$

Where we want $I_o = 1.0$mA and $I_{ref} \approx I_o$ since β is relatively large. So given that the voltage supplied is -15V at the emitter junction of the current mirror, then R, the resistances needed on the current mirror is 15kΩ.

3.1 A - Circuit and Bode Plot

The circuit is wired up as follows (figure 11). The corresponding bode plot for magnitude and phase is shown in figure 12.

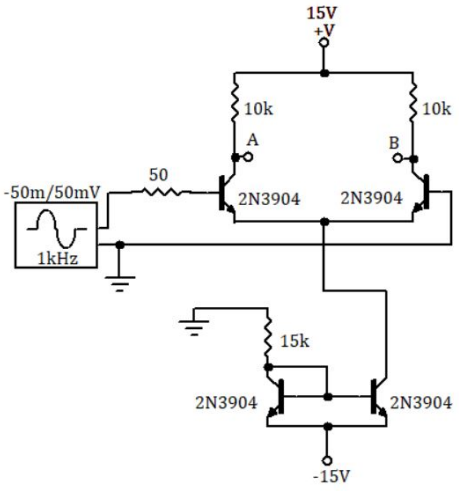
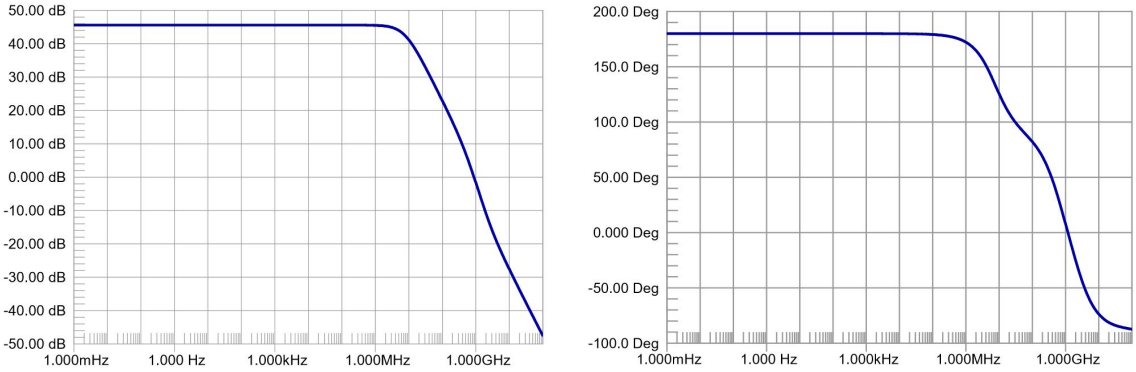


Figure 11: Differential amplifier



(a) Differential amplifier magnitude bode plot

(b) Differential amplifier phase bode plot

Figure 12: Cascaded amplifier bode plots

Using the graph, the high 3dB cut-off frequency is found to be $\boxed{7.49\text{MHz}}$.

Setting the source to a small signal of 10mV, and at a frequency of 1kHz which is at midband. The transient plot (figure 13) is used to find the amplitude of the voltage output, V_P. This is divided by the input amplitude to obtain the gain. In this sample, V_{PP} of the output signal is measured to be 3.78V. Thus,

$$|A_d| = \left| \frac{V_{PP}}{2} \times \frac{1}{V_s} \right| = \boxed{189\text{V/V}}$$

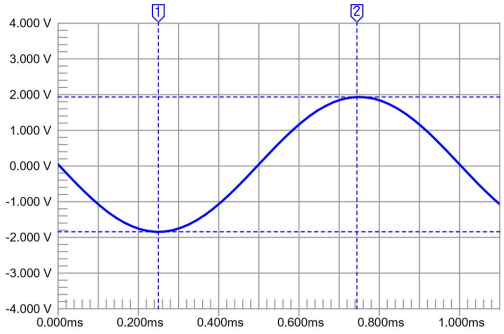


Figure 13: Transient analysis of differential amplifier

3.2 B - Frequency Response

Before we calculate any gain or frequency, we need a high-frequency small-signal model for the differential amplifier. Which is depicted in figure 14. We perform the Miller transformation, as shown in class, and we arrive at the circuit in figure 15.

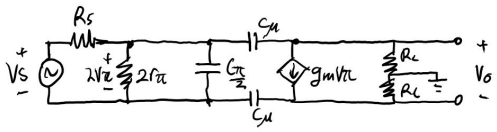


Figure 14: Differential amplifier high-frequency small signal model

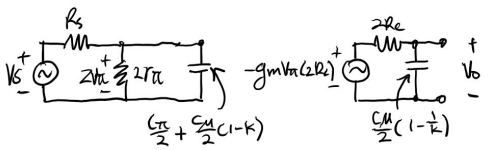


Figure 15: Differential amplifier high-frequency small signal model after Miller

Using the information we found prior: β=164, I_E=0.5mA, the base-emitter resistance, r_π is computed to be 8.2kΩ. The transconductance gain, g_m is 0.020S.

The capacitance are gathered from the data-sheet for nominal conditions. For the sake of the simplicity of the calculation, we found that C_π=8pF and C_μ=4pF.

We may proceed with computing the high frequency pole locations. Since the two capacitors after Miller transformation, as seen in figure 15, are decoupled. Calculations are straight forward and details are omitted. Here are the inverse of the pole frequencies:

$$\tau_{Hp1} = 2.03 \times 10^{-8}\text{s}, \quad \tau_{Hp2} = 4.0 \times 10^{-8}\text{s}$$

It follows that the high-frequency 3dB frequency is

$$\omega_{H3dB} = 22.3\text{Mrad}\,\text{s}^{-1} \implies f_{H3dB} = \boxed{3.55\text{MHz}}$$

To compute the gain, we consider the midband model. Which is the circuit in figure 15 except with all the capacitors treated as open circuits. It is obvious to see that

$$\frac{V_o}{V_s} = \frac{-g_m v_\pi (2R_C)}{V_s}$$

and

$$v_\pi = \frac{1}{2}\frac{2r_\pi}{2r_\pi + 50}V_s$$

Where $r_\pi = 8.2\text{k}\Omega$ as calculated earlier. Plugging everything together, we find that

$$|A_d| = \boxed{199\text{V/V}}$$

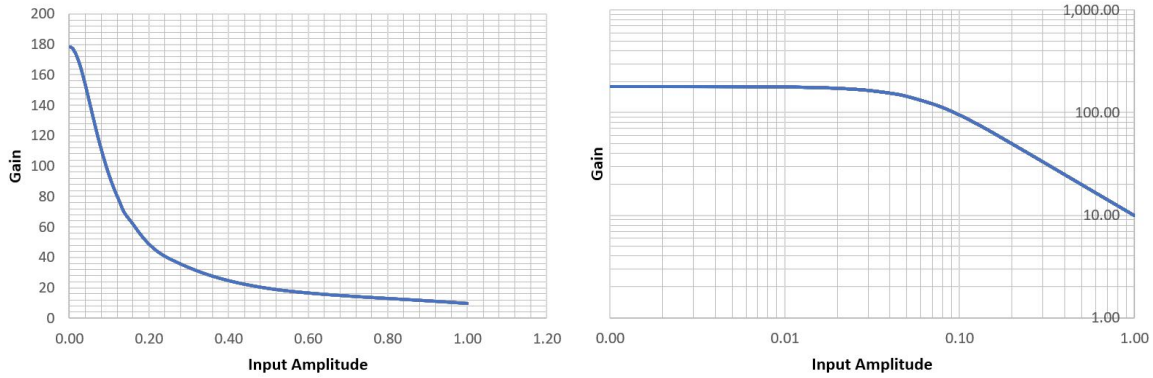
Discussion
The frequency at which the signal starts to cut off is adequate on the logarithmic scale, but inaccurate on a linear scale. This is due to the Miller effect that was imposed on the response during the Miller transformation.

The calculated gain and measured gain is very similar.

3.3 C - Saturation

Starting off with an input signal amplitude of only 1mV. The amplitude is slowly increased and the gain is sampled and recorded. The plot of gain versus input amplitude is as follows (figure 16a).

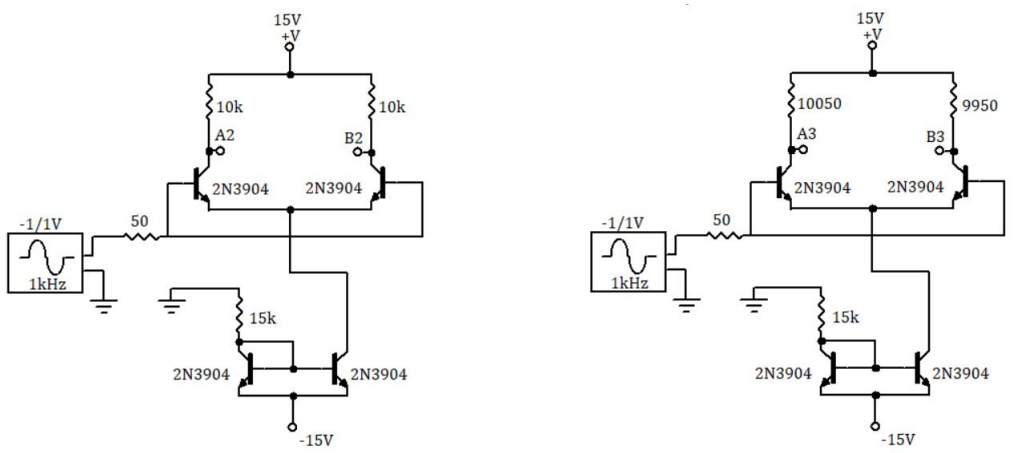
The linear region is very hard to see, and thus, hard to analyize, so I changed the axis scale to be logarithmic, as seen in figure 16b. It is much clearer to see that at around V_s=45mV, the gain becomes non-linear.



(a) Gain vs. input amplitude (b) Gain vs. input amplitude (logarithmic scale)

Figure 16: Gain vs. input amplitude as amplitude varies

3.4 D - Common-Mode



(a) Common mode differential amplifier circuit (b) Common mode with difference in R_C

Figure 17: Common mode circuits

3.4.1 No Resistance Difference

First, we hook up a common-mode signal to the differential amplifier. This means that the two base junctions of the BJTs receives the exact same, shorted, signal. The circuit is shown in figure 17a.

Note that, ideally, there is 0 gain, and thus V_o is 0V. When we measured the transient response, indeed, V_o=0V.

Calculating the common mode gain, $|A_{CM}|=\frac{\Delta R_C}{2R}$, we see that ΔR=0, thus the gain is 0, as expected. It follows that CMRR tends ∞.

3.4.2 0.5% Resistor Difference

Instead, if we do have a collector resistor difference, more specifically $\pm$0.5%at 9.95k$\Omega$and 10.05kΩ. Now the common mode gain, $|A_{CM}|=\frac{100\Omega}{2\times 15k\Omega} = 3.33\text{mV V}^{-1}$. Recall that $|A_D|$=199V/V, it follows that CMRR is

$$\text{CMRR} = 20\log_{10}\left(\frac{|3.33\times10^{-3}|}{|199|}\right) = \boxed{95.5\text{dB}}$$

3.5 E - Both Signals

When both common mode signal and differential signal are applied to the circuit, with the common mode signal amplitude to be V_P=1V at 100Hz, and differential signal at V_P=1mV at 1000Hz. The circuit is setup as shown in figure 18.

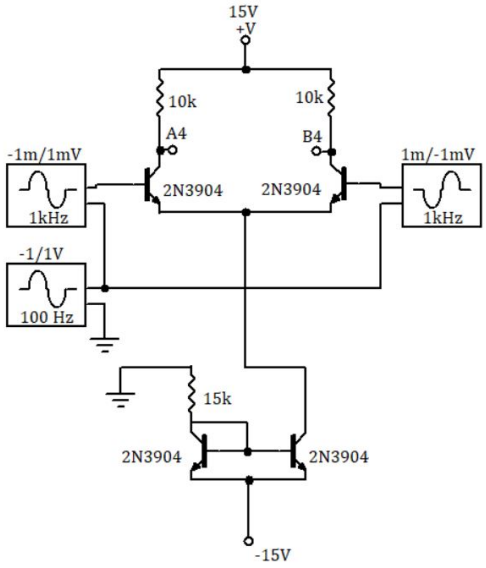
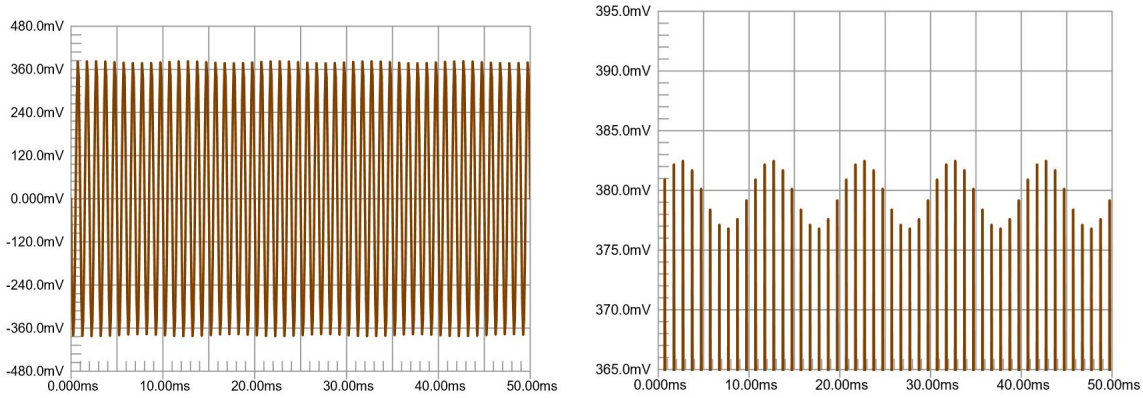


Figure 18: Both differential and common-mode signal on differential amplifier

The differential output voltage seems to look like a modulated wave (as seen in figure 19a. To see things more clearly, refer to figure 19b. We see that the wave with higher frequency is enveloped by the wave with slower frequency.



(a) (b)

Figure 19: Output voltage due to both common-mode and differential input

4 Part 4: AM Modulator

For the AM modulator, the circuit is built as shown in figure 20. Where the signal amplitude can vary between 10mV and 100mV.

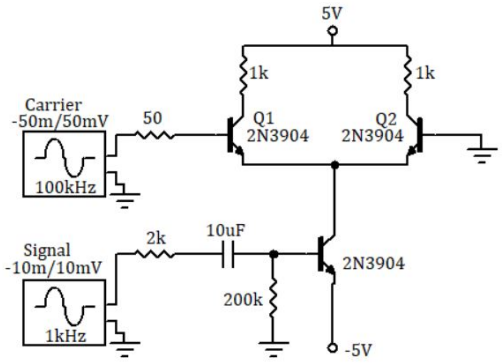


Figure 20: AM modulator circuit

4.1 A - Modulation

The output is a modulated wave (figure 21) with the carrier frequency of 100kHz and enveloped by the signal wave, which is at a relatively lower 1kHz.

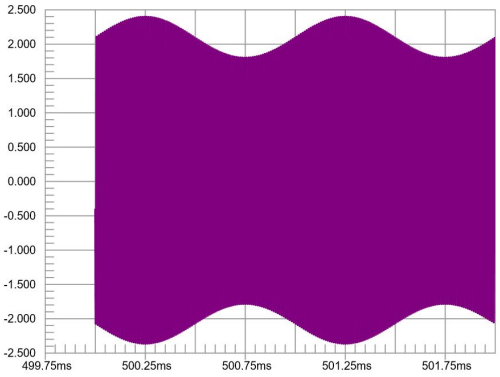


Figure 21: AM modulator modulated response

4.2 B - Saturation

I varied the input signal amplitude from 10mV to 100mV and found that at higher amplitudes, the output would be clipped / saturated, as expected from any amplifier. As the input amplitude increases, the output amplitude increases.

It is noticeable at around 85mA of input voltage amplitude, that the output starts to get distorted, as shown in figure 22.

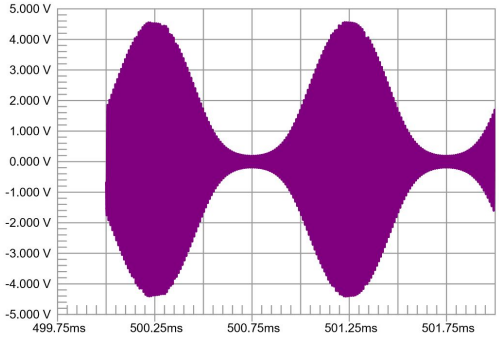


Figure 22: AM modulator output clipping

4.3 C - Square Wave

A square signal is applied instead of a sinusoidal wave, the output wave is modulated to fit the shape of the input signal, as shown in figure 23.

As input amplitude increases, output amplitude increases. When the input voltage amplitude is set to the maximum of 100mV, I noticed that the output amplitude is clipped to V_P=4V. The maximum input amplitude before the output saturates is approximately 60mV to 70mV.

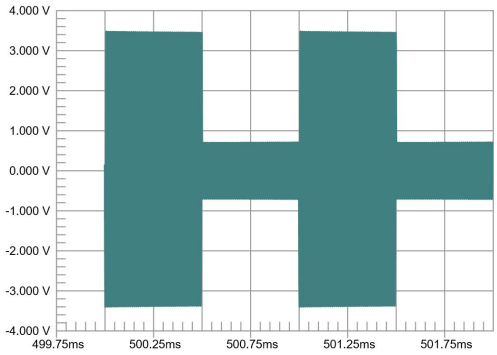


Figure 23: AM Modulation on square wave signal

Discussion
The modulator works because the input signal voltage is connected to a voltage-controlled-current source. The current source essentially dictates the gain of of the carrier wave at V_O. The carrier wave have a much higher frequency than compared to the input voltage frequency. Thus, the two waves are multiplied, and the result is amplitude modulation. An example would be if we multiply two waves with different frequency together as seen in figure 24

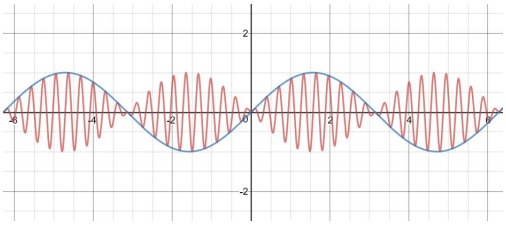


Figure 24: Two sinusoidal waves with different frequencies multiplied

5 Conclusion

In this investigation, we explored building, biasing the Cascode, cascaded, and differential amplifiers.

We learned that the Cascode amplifier has benefit of both common-emitter and common-base amplifiers as it has big input impedance for a big gain, and doesn't suffer as much from the Miller effect at high-frequencies. We learned how to use the 1/4 rule to bias the circuit, and adjusting parameters to fit the requirements needed.

We learned the applications of cascaded amplifier as a repeater in signal transferring systems.

We learned to use differential amplifier, its model, and how to bias it. In fact, we learned how modulation worked, and how to implement one using the differential amplifier.

Finally, we learned that we should start the mini-project sooner so we're not pulling last-minute changes.

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