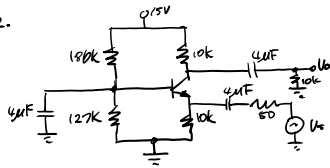


Problem Set 4 (Again)

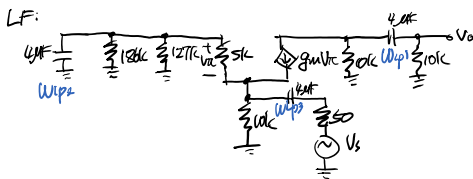
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Q2.



Biasing:

$V_{BB} = 6.086V$
 $R_{BB} = 75.47k$
 KVL: $V_{BB} = I_B \cdot R_{BB} + 0.7 + (1+\beta)I_B \cdot 10k$
 $\rightarrow I_B = \frac{V_{BB} - 0.7}{R_{BB} + (1+\beta)10k} = 4.762\mu A$
 $I_C = \beta I_B = 0.496mA$
 $I_E = 0.501mA$
 $g_m = 0.01995V$
 $r_E = \frac{100}{g_m} = 5k\Omega$



$$W_{LP1} = (4\mu F \cdot (20k))^{-1} = 12.5 \text{ rad/s}$$

— SCLC test (looking for big trap):

$\tau_{SC} = 4\mu F \cdot [180k \parallel 120k \parallel (5k + (1+\beta)(10k \parallel 150k))]$
 $= 0.095s$
 $W_{LP2} = 28.25 \text{ rad/s}$
 $\tau_{SC} = 4\mu F \cdot [(1+\beta)(5k \parallel 10k) + 50]$
 $= 3.97 \times 10^{-4}s$
 $W_{LP3} = 2517 \text{ rad/s}$

— DC test

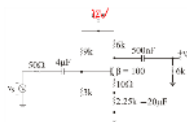
$\tau_{DC} = 4\mu F \cdot [180k \parallel 120k \parallel 5k + (1+\beta)10k]$
 $= 0.281s$
 $W_{LP2} = 3.56 \text{ rad/s}$

$$W_{LP2} = \frac{1}{4\mu F (180k \parallel 120k)} = 33 \text{ rad/s}$$

$$W_{3dB} = 2517 \text{ rad/s}$$

3) For the circuit shown in Figure 3:

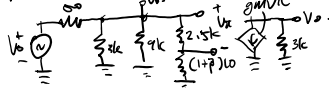
- Draw the low-frequency circuit, the midband circuit and the high-frequency circuit and
- Derive the midband gain, A_m , and $F_u(f)$.



Bias Conditions:

$V_B \approx 3V$ since $I_1 \gg I_B$
 $V_E = 2.3V, I_E = \frac{2.3V}{2.2k} \approx 1mA$
 $I_C \approx 1mA$
 $I_B = \frac{I_C}{\beta} = 10\mu A, I_2 = 1mA$
 $g_m = \frac{I_C}{V_T} = \frac{1mA}{25mV} = 0.04V$
 $r_E = \frac{100}{g_m} = 2.5k\Omega$

MB:



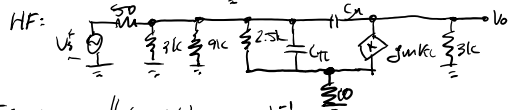
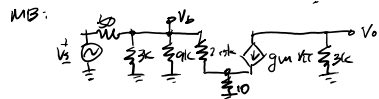
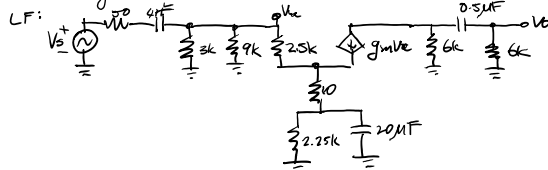
$$V_{TC} = V_B - V_E, \quad V_{TC} = I_E \cdot 10k = I_B \cdot (1+\beta)(10k)$$

$$\text{Voltage divider: } V_B = \frac{3k \parallel 10k \parallel (2.5k + (1+\beta)10k)}{3k \parallel 10k \parallel (2.5k + (1+\beta)10k) + 50} \cdot 12V$$

$$V_B = 0.965V$$

$$I_B = \frac{V_B}{10k}$$

Small Signal Model



$$LF: W_{LP1} = (6k \parallel 6k \cdot 0.5\mu F)^{-1} = 167 \text{ rad/s}$$

DC test (want low freq)

$$\tau_{DC} = 4\mu F \cdot (50 \parallel 3k \parallel 1k \parallel (2.5k + (1+\beta)(10 \parallel 2.2k))) = 0.091s \quad \checkmark \rightarrow W_{LP2} = 109 \text{ rad/s}$$

$$\tau_{DC} = [(3k \parallel 1k) + 7.5k] \cdot (1+\beta) \cdot 10 \parallel 2.2k \cdot 20\mu F = 0.002s \quad \times$$

SCLC test:

$$\frac{2k // 9k // (2.5k + 4.7k) + 50}{2k // 9k // (2.5k + 4.7k) + 50} = 0.0023 \times$$

$$V_b = 0.95V_s$$

$$i_b = \frac{V_b}{2k + (1 + \beta)10k} = 2.749 \times 10^{-4} A$$

$$V_{\pi} = 0.95V_s - (2.749 \times 10^{-4})V_b \cdot (1 + \beta)(10k)$$

$$V_{\pi} = 0.687V_s$$

$$V_o = -g_m V_{\pi} (5k)$$

$$= -0.04 \cdot 0.687 V_s \cdot 3k$$

$$\frac{V_o}{V_s} = -81.44$$

SCTC test.

$$\tau_{sc}^{CE} = \left[\left((50 + 2.5k) \cdot \left(\frac{1}{1 + \beta} \right) + 10 \right) // 2.5k \right] \cdot 20\mu F$$

$$= 0.694 \times 10^{-3} s$$

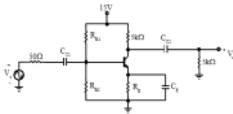
$$W_{LP3} = 1441 \text{ rad/s}$$

$$W_{L21} = W_{L22} < 0.$$

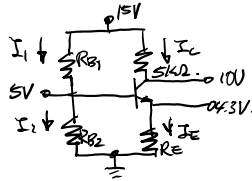
$$W_{L23} = \frac{1}{R_E \tau_E} = 22.2 \text{ rad/s}$$

$$F_L(s) = \left(\frac{s}{s + 167} \right) \left(\frac{s}{s + 109} \right) \left(\frac{s + 22.2}{s + 1441} \right)$$

4) For the circuit shown in figure 4, use the 1/3rd rule (your choice) to bias the circuit and find C_E , C_{C1} , and C_{C2} that will put the low frequency poles at 1000/s, 100/s and 10/s. Choose the lowest cost combination of capacitors.



Using the first 1/3 rule: $V_B = \frac{1}{3}V_{CC}$, $V_C = \frac{2}{3}V_{CC}$, $I_1 = \frac{I_E}{\beta}$, $\beta = 100$.



$$V_C = 10V, V_B = 5V, V_E = 4.3V$$

$$I_E = \frac{5V}{5k} = 1mA$$

$$I_B = \frac{I_E}{\beta} = 10\mu A$$

$$I_E = 1.01mA$$

$$I_1 = \frac{1.01mA}{10} = 101\mu A$$

$$I_2 = I_1 - I_B = 91\mu A$$

$$R_E = \frac{4.3V}{1.01mA} = 4.26k\Omega$$

$$R_{B1} = \frac{15-5V}{101\mu A} = 99k\Omega$$

$$R_{B2} = \frac{5V}{91\mu A} = 54.95k\Omega$$

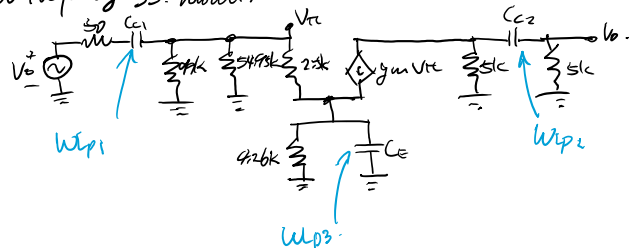
For the best cost efficiency, C_{C2} should short first, C_{C1} should short second, C_E should short last.

Thus 10/s corresponds to C_{C1} , 100/s corresponds to C_{C2} , 1000/s corresponds to C_E .

$$g_m = \frac{I_E}{V_T} = \frac{1mA}{25mV} = 0.0402$$

$$V_{\pi} = \frac{V}{g_m} = 2.5k\Omega$$

Low Frequency SS. model:



$$\text{First } W_{LP1} = (C_{C2} \cdot (5k + 5k))^{-1} = 100/s$$

$$C_{C2} = \frac{(10)}{10k} = 1\mu F$$

Next, with R_E open (OCTC test), we have

$$W_{LP2} = \{C_{C1} \cdot [50 + 99k // 54.95k // ((4.7k // 2.5k) + 2.5k)]\}^{-1} = 10/s$$

$$\Rightarrow C_{C1} \cdot [...] = \frac{1}{10s}$$

$$\Rightarrow C_{C1} = 3.06\mu F$$

Lastly, with all capacitors shorted (SCTC test), we have

$$\tau_{sc}^{CE} = \frac{1}{W_{LP3}} = \frac{1}{1000s} = C_E \cdot \left[\left((50 // 99k // 54.95k) + 2.5k \right) \left(\frac{1}{1 + \beta} \right) // 4.26k \right]$$

$$\Rightarrow C_E = 39.843\mu F$$