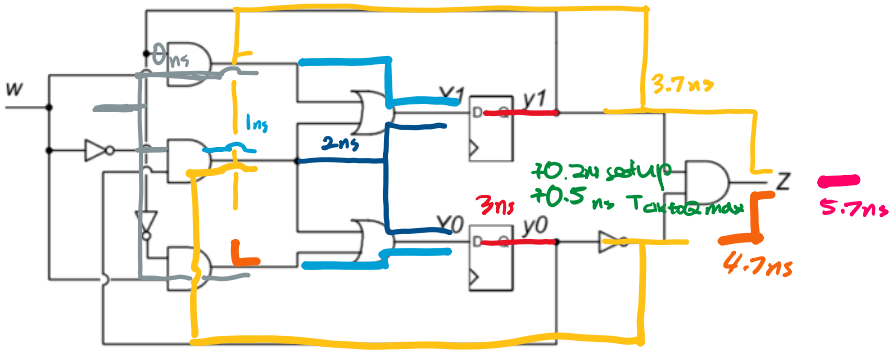
Ps4

April 9, 2018 10:31

1. Consider the following circuit. The clock connections to the flip-flops are not shown (both flip-flops are clocked by the same clock).



Assume the following:

Delay of each logic gate: 1 ns
Set up time of each flip-flop: 0.2 ns
Hold time of each flip-flop: 0 ns
Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
Minimum Clk-to-Q delay of each flip-flop: 0.1 ns

a) What is the maximum frequency of the clock in this circuit (in Mhz) ?

The critical path takes 5.7ns. However, the delay in logic blocks at the end don't matter.

Thus the maximum clock frequency is:

$$f_{max} = \frac{1}{3.7ns} = \boxed{270.27\,MHz}$$

b) Suppose the hold time is not 0. What is the largest value for the hold time for which this circuit will still function properly?

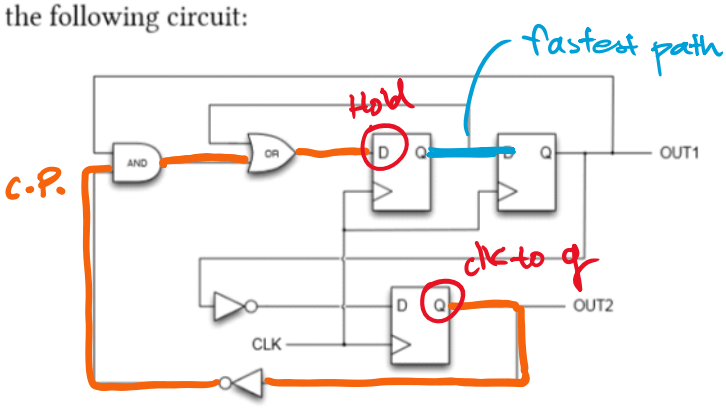
$$t_{clk\text{-}to\text{-}q} + t_{s\,path} \geq t_{hold}$$

Shortest path (from reg through two gates):

$$0.1 + 2(1) = \boxed{2.1ns}$$

(min. clk to q)

2. Consider the following circuit:



Assume the following:

- Delay of each inverter: 0.6 ns
- Delay of each AND and OR gate: 1 ns
- Set up time of each flip-flop: 0.3 ns
- Hold time of each flip-flop: 0.2 ns
- Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
- Minimum Clk-to-Q delay of each flip-flop: 0 ns

Answer the following questions:

a) What is the maximum frequency of this circuit (in Mhz) ?

Max delay in critical path:

$2(1) + (0.3 + 0.5) + 1(0.6)$

(setup time; max clk-to-q time)

$= 3.4\text{ns}$

$F_{max} = \frac{1}{3.4\text{ns}} = \boxed{294\text{MHz}}$

b) Suppose the minimum Clk-to-Q delay is not 0 ns. What is the smallest value of the minimum Clk-to-Q delay such that there is no hold time violation in this circuit?

Recall that hold time violation happens when delay in fastest path < hold time.

Delay in fastest path: NO logic delays + FF delay

$\Rightarrow$ thus the minimum clk-to-q delay > hold time.

clk-to-q time > $\boxed{0.2\text{ns}}$

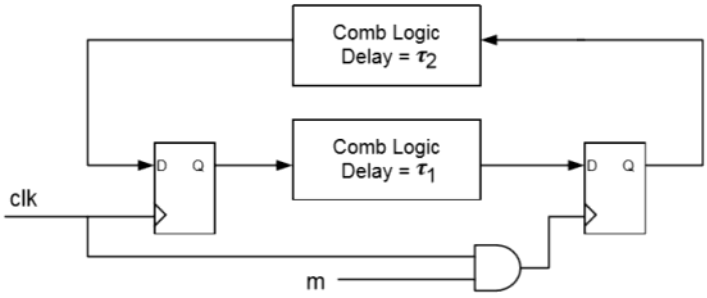
3. Suppose a high-end microprocessor is to run at 2Ghz (remember than 2Ghz = 2000 Mhz). Further, suppose the delay of each logic gate is 0.08 ns. Assume the set-up, hold, and Clk-to-Q times of all flip flops are 0. What is the maximum number of gates that can appear in the critical path of this circuit? (note: all the numbers in this question are realistic, and the answer has a huge effect on the logic design of high-end microprocessors... you'll learn more about this in CPEN 411 if you take it).

Maximum time allowed per cycle = $\frac{1}{2\text{Ghz}}$

$= 0.5\text{ns}$

$\left\lfloor \frac{0.5\text{ns}}{0.08\text{ns}} \right\rfloor = \boxed{6 \text{ logic gates}}$

4. Consider the following circuit. Note that the second flip-flop's clock input is derived from the clock signal and input signal m (so the clock only goes high when m is high).



Assume the following:

Set up time of each flip-flop: 0.3 ns
Hold time of each flip-flop: 0.2 ns
Maximum Clk-to-Q delay of each flip-flop: 0.5 ns
Minimum Clk-to-Q delay of each flip-flop: 0.25 ns
Delay of the AND gate: 1 ns

Suppose we want to run this circuit at 100 Mhz. Answer the following questions:

a) What is the ***maximum*** possible value of τ_1 that the circuit is guaranteed to work correctly at 100 Mhz? Show your work. If there is no maximum, write ∞.

→ At 100MHz, the period is $\frac{1}{100\text{MHz}} = 10\text{ns}$

Because destination FF is driven by a derived clock, the AND gate added 1.0ns slack

total time = 11 ns

→ the path that goes through τ_1 also needs account for clk to q time at source FF and hold time at dest. FF

$\tau_1 + 0.3\text{ns} + 0.25\text{ns} = 11\text{ns}$

τ_1: maximum; 0.25ns: maximum clk to q

$\boxed{\tau_1 = 10.2\text{ ns}}$

b) What is the ***maximum*** possible value of τ_2 for the circuit to work correctly at 100 Mhz? Show your work. If there is no maximum, write ∞.

Since the clock on second FF fires later, we reduced τ_2 slack by 1ns

$$\tau_2 + 0.3ns + 0.5ns = 9ns$$

$$\boxed{\tau_2 = 8.2\,ns}$$

c) What is the ***minimum*** possible value of τ_1 for the circuit to work correctly at 100 Mhz? Show your work. If there is no minimum, write 0.

Normally: the minimum time is:

hold time − clk to q min

In this case, the clock will arrive 1ns late thus

$$\tau_{1\,min} = t_{hold} - t_{clk\,to\,q\,min} + 1ns$$
$$= 0.2 - 0.25 + 1$$
$$= \boxed{0.95ns}$$

d) What is the ***minimum*** possible value of τ_2 for the circuit to work correctly at 100 Mhz? Show your work. If there is no minimum, write 0.

Normally this would be hold time − clk to q min time < 0

In addition to the clock skew, $= \boxed{0}$ still